16-Bit MOTHER BOARD
USERS MANUAL

CONTENTS

SECTION I

PC/XT System Board

The PC/XT system board fits horizontally in the base of the system unit and is approximately 8 1/2 12 inches. It is a double sided P.C.B. DC power and a signal from the power supply enter the board through two six-pin connectors. Other connectors on the board are for attaching the keyboard and speaker. Eight 62-pin card edge-sockets are also mounted on the board. The I/O channel is bussed across these eight I/O slots.

A dual-in-line package (DIP) switch (SWI) (one eightswitch pack) is mounted on the board and can be read under program control. The DIP switch provides the system software with information about the installed options, how much storage the system board has, what type of the display adapter is install-led, what operation modes are desired when power is switched on (color or black-and-white, 80-or 40-character lines), and the number of diskette drive attached.

The system board consists of five functional area: the processor subsystem and its support elements, the read-only mormory (ROM) subsystem, the read/write (R/W) memory subsystem, integrated I/O adapters, and the I/O channel. All are desired in this section.

The heart of the PC/XT system board is the Intel 8088 micro-processor. This pocessor is an 8-bit external bus version of Intel's 16-bit 8086 processor, and is software-compatible with the 8086. Thus, the 8088 supports 16-bit operations, including multiply and divide, and supports 20 bits addressing (1 megabyte of storage). It also operates in maximum mode, so a coprocessor can be added as

a feature. The processor operates at a 4.77 MHz. This frequency, which is derived from a 14.318 MHz crystal, is divided by 3 for the processor clock, and by 4 to obtain the 3.58 MHz color burts signal required for color televisions.

At the 4.77 MHz clock rate, the 8088 bus cycles are four, clocks of 210 ns, or 840 ns. I/O cycles take five 210 ns clocks or 1.05 microseconds.

The processor is supported by a set of high-function support devices providing four channels of 20-bit direct-memory access (DMA), three 16-bit timer-counter channels, and eight prioritized interrupt levels.

Three of the four DMA channels are available on the I/O bus and support high speed data transfers between I/O devices and memory without processor intervention. The fourth DMA channel is programmed to refresh the system dynamic memory. This is done by programming a channel of the timer-counter device to periodically request a dummy DMA transfer. This action creates a memory-read cycle, which is available to refresh dynamic storage both on the system board and in the system expansion slots. All DMA data transfers, except the refresh channel, take five procesor clocks of 210 ns, or 1.05 us if the processor-ready line is not deactivated. Refresh DMA cycles take four clocks or 840 ns.

The three programmable timer/counters are used by the system as follows: Channel 0 is used as a general-purpose timer providing a constant time base for implementing a time-of-day clock; Channel 1 is used to time and request refresh cycles from the DMA channel; and Channel 2 is used to support the tone generation for the audio speaker. Each channel has a minimum timing resolution of 1.05 us.

Of the eight prioritized levels of interrupt, six are bussed to the system expansion slots for use by features card. Two levels are used on the system board. Level 0, the high- est priority, is attached to Channel 0 of the time/counter and provides a periodic interrupt for the time-of-day clock. Level 1 is attached to the keyboard adapter circuits and receives an interrupt of each scan code sent by the keyboard. The non-maskable interrupt (NMI) of the 8088 is used to report memory parity errors.

The system board supports both ROM/EPROM and R/W memory. It has space for 128K x 8 of ROM or EPROM. This ROM contains the power-on self-test, I/O drivers, dot patterns for 128 characters in graphics mode, and a diskette and has an access time and a cycle time of 250 ns each.

The system board also has from 128KB to 256KB of R/W memory. A minimum system would have 128K of memory, with module sockets for an additional 128K. Memory greater than the system boards maximum of 256K is obtained by replacing The 4164 Memory IC to 41256 on Bank 0 and Bank 1, and short the jumper 1.

The system board contains the adapter circuits for attaching the serial interface from the keyboard. These circuits generate an interrupt to the processor when a complete scan code is received. The interface can request execution of a diagnostic test in the keyboard.

The keyboard interface is a 5-pin DIN connector on the system board that extends through the rear panel of the system nuit.

The system units has an 2-1/4 inch audio speaker. The speaker's control circuits and driver are on the system board. The speaker connects through a 2-wire interface that attaches to a 3-pin connector on the system board.

The speaker drive circuit is capable of approximately 1/2 watt of power. The control circuits allow the speaker to be driven three different ways: 1) a direct program control register bit may be toggled to generate a pulse train; 2) the output from Channel 2 of the timer counter may be programmed to generate a waveform to the speaker; 3) the clock input to the timer counter can be modulated with a program-controlled I/O register bit. All three methods may be performed simultaneously.

SECTION II

I/O Channel

The I/O channel is an extension of the 8088 microprocessor bus. It is, however, demultiplexed, repowered, and enhance by the addition of interrupts and direct memory access (DMA) functions.

The I/O channel contains a

The I/O channel contains an 8 bit, bidirectional data bus, 20 address lines, 6 levels of interrupt, control lines for memory and I/O read or write, clock and timing lines, 3 channels of DMA control lines, memory refresh timing control lines, a channel check line, and power and ground for the adapters. Four voltage levels are provided for I/O cards: +5 Vdc, -5dc, +12 Vdc, and -12dc. These functions are providccded in a 62-pin connector with 100-mil card tab spacing.

A ready line is available on the I/O channel to allow operation with slow I/O or memory devices. If the channel's ready line is not activated by an addressed device, all processor-generated memory read and write cycles take four 210-ns clock or 840-ns/byte. All processor-generated I/O read and write cycles require five clocks for a cycle time of 1.05 us/byte. Refresh cycles occur once every 72 clocks (approximately 15 us) and require four clocks or approximately 7% of the bus bandwidth.

I/O devices are addressed using I/O mapped address space. The channel is designed so that 768 I/O device addressed are available to the I/O channel cards.

A channel check line exists for reporting error conditions to the processor. Activating this line results in a Non-Maskable Interrupt (NMI) to the 8088 processor. Memory expansion options use this line to report parity errors.

The I/O channel is repowered to provide sufficient drive to power all eight (J1 through J8) expansion slots, assuming two Low-Power Sohorttky (LS) loads per slot. The I/O adapters typically use only one load.

SECTION III

I/O Channel Description

The following is a description of the PC/XT I/O Channel. All lines are TTL-compatible.

Signal I/O Description

OSC O Oscillator:

High; speed clock with a 70-ns period (14.31818 MHz). It has a 50% duty cycle.

CLK O System Clock:

It is a divide-by-three of the oscillator and has a period of 210 ns (4.77 MHz). The clock has a 33% duty cycle.

RESET DRV O:

This line is used to reset or initizlize system logic upon power-up or during a low line voltage outage. This signal is synchronized to the falling edge of clock and is active high.

AO-A19 O Address Bitss 0 to 19:

These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. AO is the least significant bit (LSB) and A19 is the most significant bit (MSB). These lines are generated by either the processor or DMA controller. They are active high.

DO-D7 I/O Data Bits 0 to 7:

These lines provide data bus bits 0 to 7 for the processor, memory, and I/O devices. DO is the least significant bit (LSB) and D7 is the most significant bit (MSB). These lines are actibe high.

ALE O Address Latch Enable:

This line is provided by the 8288 Bus Controller and is used on

the system board to latch valid addresses from the processor. It is available to the I/O channel as an indicator of a vilid processor address (when used with AEN). Processor adresses are latched with the failing edge of ALE.

I/O CH CK-I I/O Channel Check:

This line provides the processor with parity (error) information on memory or devices in the I/O channel. When this signal is active low, a parity error is indicated.

I/O CH RDY I I/O Channel Ready:

This line, normally high (ready), is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a read or write command. This lines should never be held low longer than 10 clock cycles. Marchine cycles (I/O or memory) are extended by an integral number of CLK cycles (210 ns).

IRQ2-IRQ7 I Interrupt Reguest 2 to 7:

These lines are used to signal the processor that an I/O device reguires attention. They are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. An Interrupt Reguest is generated by raising an IRQ line (low to high) and holding it high until it is acknowledged by the processor (interrupt service routine).

IOR O I/O Read Command:

This command line instructs an I/O device to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

IOW O I/O Write Command:

This command line instructs an I/O device to read the data on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

MEMR O Memory Read Command:

This command line instructs the memory to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

MEMW O Memory Write Command:

This command line instructs the memory to store the data presen on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

DRQ-DRQ3 I DMA Request 1 to 3:

These lines are asynchronous channel requests used by peripheral devices to gain DMA service. They are prioritized with DRQ3 being the lowest and DRQ1 being the highest. A request is generated by bringing a DRQ line to an active level (high). A DRQ line must be held high until the corresponding DACK line goes active.

DACKO – 3 O DMA Acknowledge 0 to 3:

These lines are DACK3 used to acknowledge DMA requests (DRQ1-DRQ3) and to refresh system dynamic memory (DACKO). They are active low.

AEN O Address Enable:

This line is used to degate the procesor and other devices from the I/O channel to allow DMA transfers to take place. When this

line is active (high), the DMA controller has control of the address bus, data bus, read command lines (memory and I/O), and the write command lines (memory and I/O).

T/C O Terminal Count:

This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active high.

CARD SLCTD I Card Selected:

This line is activated by cards in expansion slot J8. It signals the system board tat the card has been selected and that appropriate drivers on the system board should be directed to either read from, or write to, expansion slot J8. Connectors J1 through J8 are tied together at this pin, but the system board should be driven by an open collector device.

The following voltages are available on the system-board I/O channel:

+5 Vdc +– 5%, located on 2 connector pins
-5 Vdc +–10%, located on 1 connector pin
+12 Vdc +– 5%, located on 1 connector pin
-12 Vdc +–10%, located on 1 connector pin
GND (Ground), located on 3 connector pins

SECTION IV

Speaker Interface

The sound system has a small, permanent-magnet, 2-1/4 inch speaker. The speaker can be driven from one or both or two sources:

* An 8255A-5 PPI output bit. The address and bit are difined in the "I/O Address Map".

* A timer clock channel, the output of which is programmble within the functions of the 8253-5 timer when using a 1.19-MHz clock input. The timer gate also is controlled by an 8255A-5 PPI output-port bit. Address and bit assignment are in the "I/O Address Map".

The speaker connection isa 4-pin berg connector. See "System Board Component Diagram", earlier in this section, for speaker connection or placement.

SECTION V

PC/XT System Board Switch Setting

The DIP Switch (SW1) located at U20 is used to set the system configration and to specify the amount of memory installed on the system board.


```
The Switch setting as follows:
  Position    Function
     1        Normal operation off
     2        Use for 8087 Coprocessor
    3-4       Amount of memory on system board
    5-6       Type of display adapter
    7-8       Number of 5-1/4 inch drives

Switch (SW1):
    1=OFF (NORMAL OPERATION)
    2=ON W/O 8087 co-processor
    2=OFF W/ 8087 co-processor

Memory Switch Settings:
       [ 256K Type ]
    3=OFF 4=ON   128K MEMORY INSTALLED
    3=ON  4=OFF  192K MEMORY INSTALLED
    3=OFF 4=OFF  256K MEMORY INSTALLED
       [ 640K Type ]
    3=OFF 4=ON   512K MEMORY INSTALLED
    3=ON  4=OFF  576K MEMORY INSTALLED
    3=OFF 4=OFF  640K MEMORY INSTALLED

Display Adapter Switch Settings:
    5=ON  6=ON   No Display Adapter
    5=OFF 6=ON   Color/Graphics (40x20
                 Mode)
    5=ON  6=OFF  Color/Graphics (80x25
                 Mode)
    5=OFF 6=OFF  Monochrome Display Adapter
                 or both

Display Drive Switch Setting:
    7=ON  8=ON   1 Drive Installed
    7=OFF 8=ON   2 Drives Installed
    7=ON  8=OFF  3 Drives Installed
    7=OFF 8=OFF  4 Drives Installed
```

7 = ON 8 = OFF 3 DRIVES INSTALLED

7 = OFF 8 = OFF 4 DRIVES INSTALLED

SECTION VI

PC/XT EPROM/ROM Switch Settings:

The Super XT board will accept 4 different type of ROM/EPROM for the system memory.

The switch settings are as follow:

W	1	2	3	4	5	6	7	8	9	10	11	12
2764 EPROM	1	0	1	0	1	0	1	0	0	1	0	1
27128 EPROM	1	0	0	1	1	0	1	0	1	0	0	1
8Kx8 ROM	1	0	1	0	0	1	0	1	0	1	0	1
32Kx8 ROM	0	1	0	1	1	0	1	0	1	1	1	0

NOTE: 1 = ON 0 = OFF

W1 – W8 is located next to U35 (ROM 7)
W9 – W1 is located above U24 (74LS02)

The memory decoder (U23 & 74LS02) must position in the right place as follows:

Position A: 2764 EPROM or 8Kx8 ROM
B: 27128 EPROM
C: 32Kx8 ROM

NOTE: EPROM's pin out must be Intel compatible with access time not more than 250ns. ROM7 has the highest address.

SECTION VII

Power Up Reset Jumper: (JP1)

The Super XT board will accept 4 different type of ROM/EPROM power supply PIN 1. If use an IBM power supply, insert a jumper on, JP1 from 1 to 2, otherwise, connect Jumper JP1 from 2 to 3 which will provide a power up reset circuit on board.

SECTION VIII

Some Trouble Shooting Points

This section give some hints to experienced engineers and technicians to test and bring up the Super XT system board.

(1) System Clock:
4.77 MHz at U1 (8284A) PIN 8 and &3 (8088) PIN 10, etc., with 33% duty cycle. If no system clock, check Y1 (14.318MHz) crystal, U1.

(2) Power Up Reset:
When power up &3 (8088) PIN 21 should go HIGH then back to low again. If no power up, please check jumper on JP1.

(3) Memory Decoding Circuit:
When power up, the processor will start execute the program through ROM 7 (BIOS & Self Test). The CS7 – line should

see a train low again pluses to fetch instruction from the ROM 7. If no pulses on CS7 – on U23 (LS138 PIN 7), check the memory decoding circuit and make sure the ROM/EPROM Jumpers (W1-W12) are in the right position.

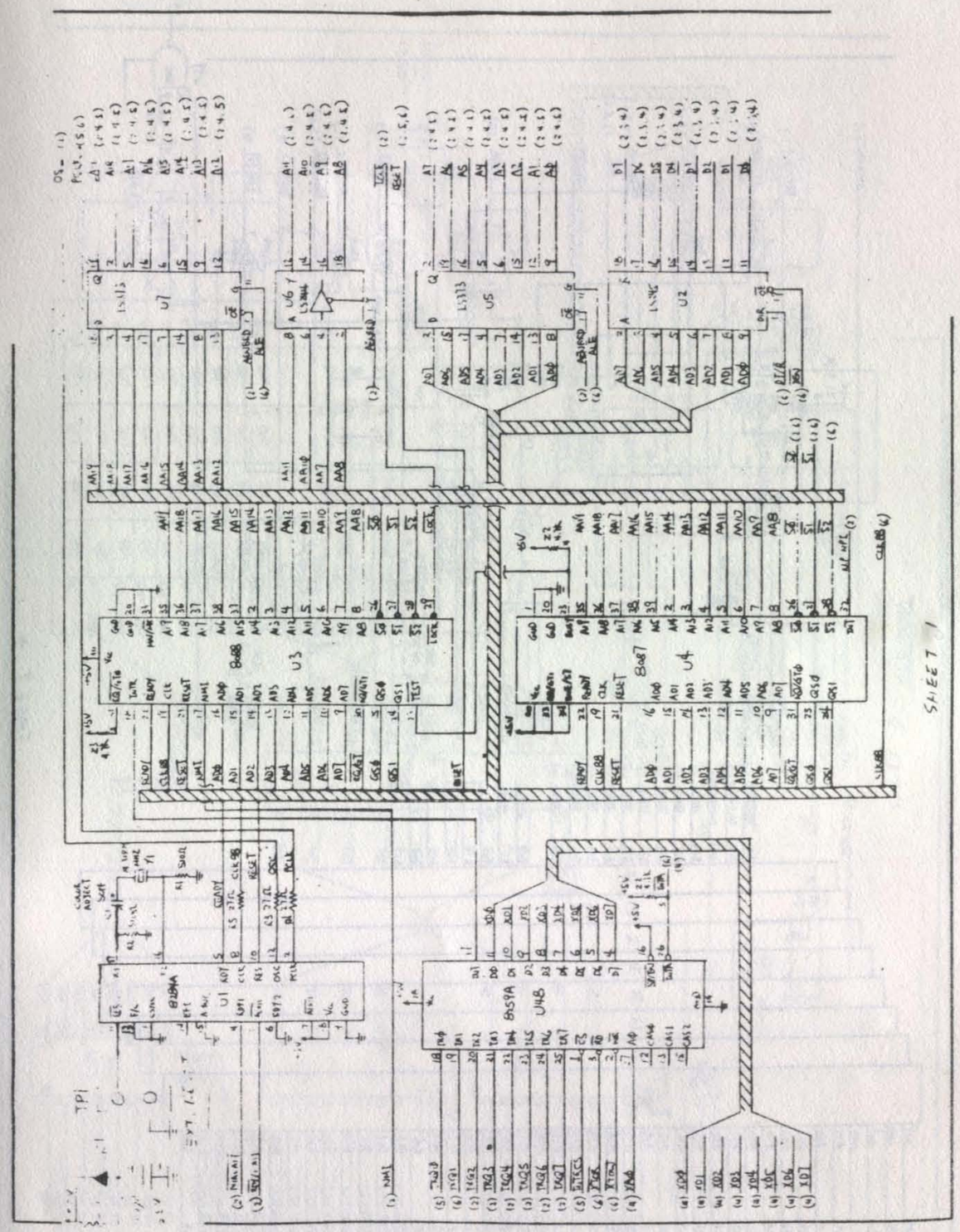
(4) RAM Refresh:
The RAM is being refresh using the timer chip U49 (8253-5 PIN 13 OUT 1) to trigger the chip (8237A-5 DRQO, and the DMA chip will send out a dummy address to refresh the dynamic RAMs (4164). If no periodic low pulses on RAM chip PIN 4 (RAS-), check the TIMER, DMA, and refreshing circuit.

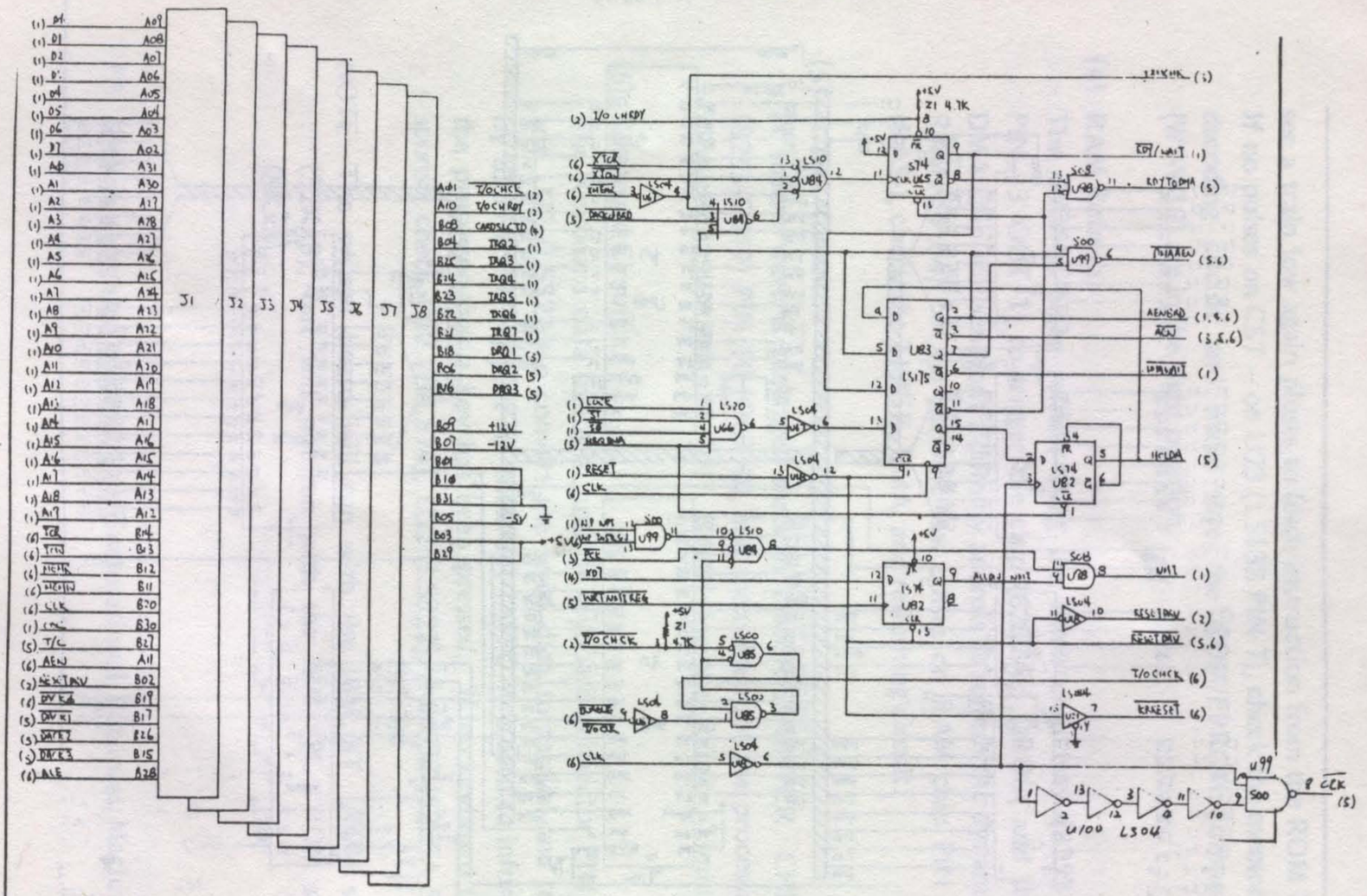
(5) R.T.C. Circuit:
A square wave is generated through TIMER/COUNTER CHIP (8253-5U49) PIN 10 (OUT 0), and then interrupt the processor through 8259A PIN 17 (INT Signal) for the R.T.C. Timing.

(6) Keyboard Circuit:
The Keyboard data input is through keyboard connector PIN 2 and U22 (LS322) to convert the serial data to parallel and red by 8255A-5 (U37) port A. Interrupt 1 (ITQ 1) is used to inform the processor that a key has been pressed. If no keyboard response, check U52 (74LS74), U22 (LS322), and U37 (8255A-5).

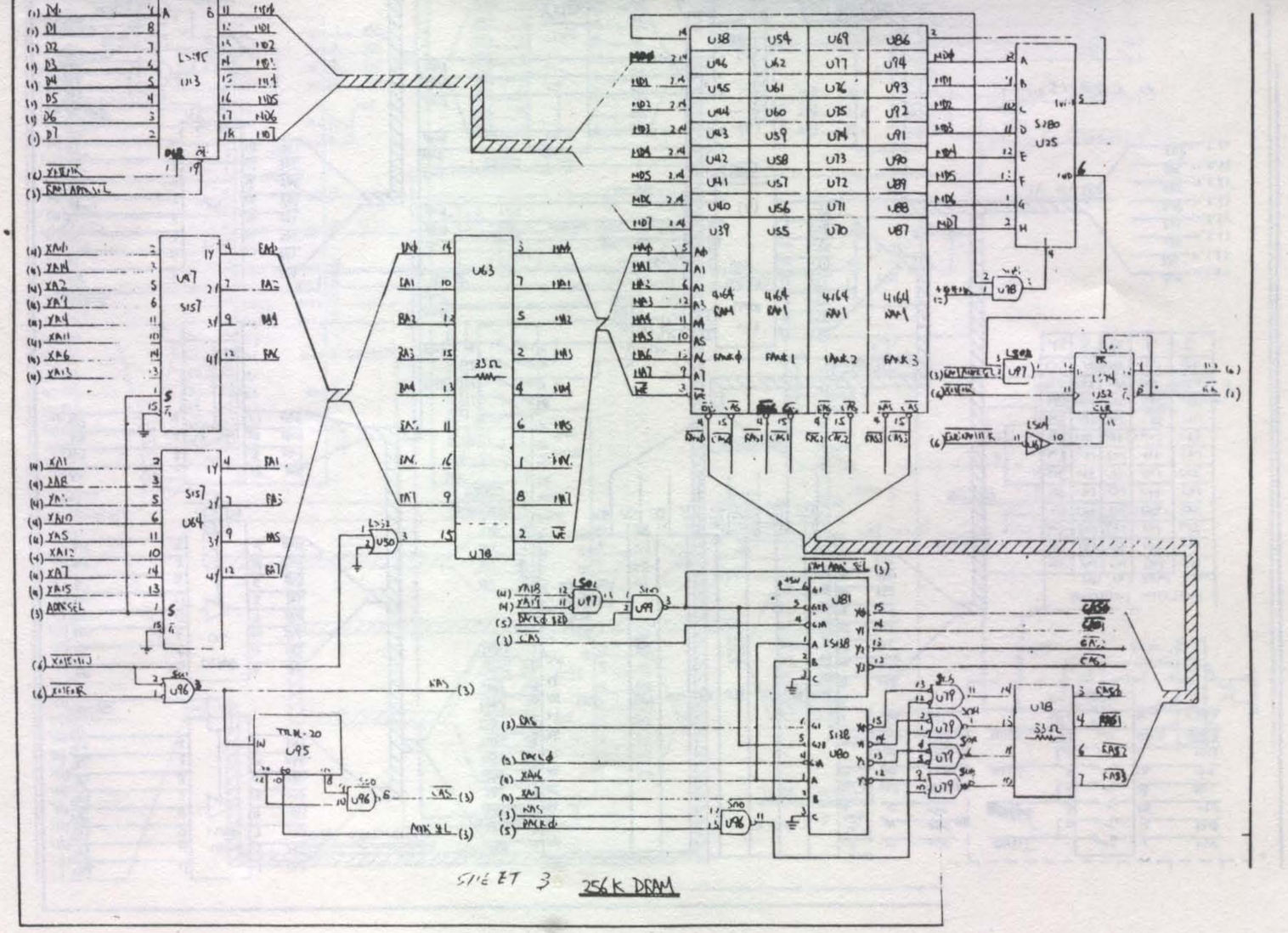
NOTE: The system board will run with the IBM XT ROM set (32Kx8), but will not run with the IBM PC ROM set (8Kx8).

** IBM is a register trademark of International Bussiness Machine Corp.

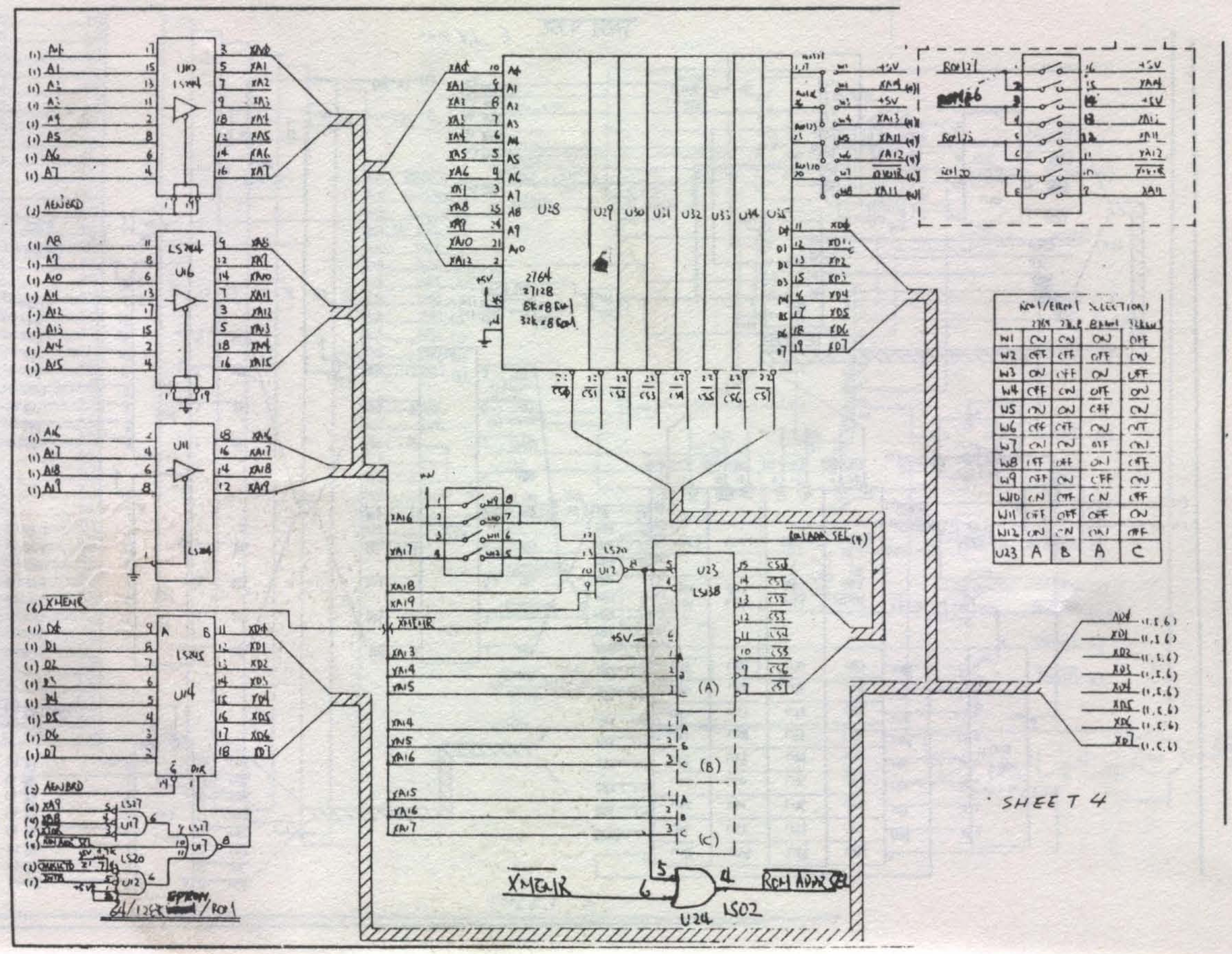




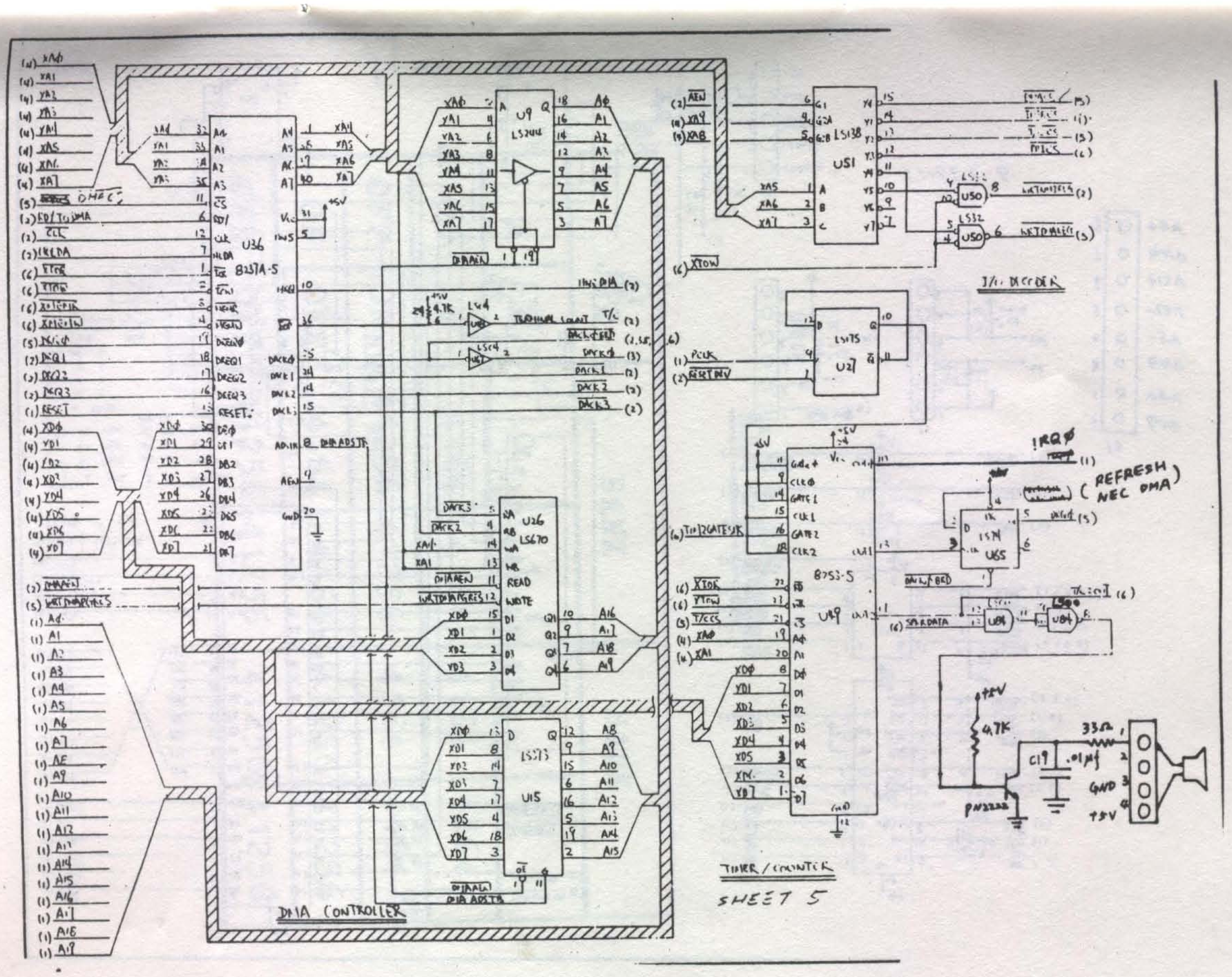
SHEET 2

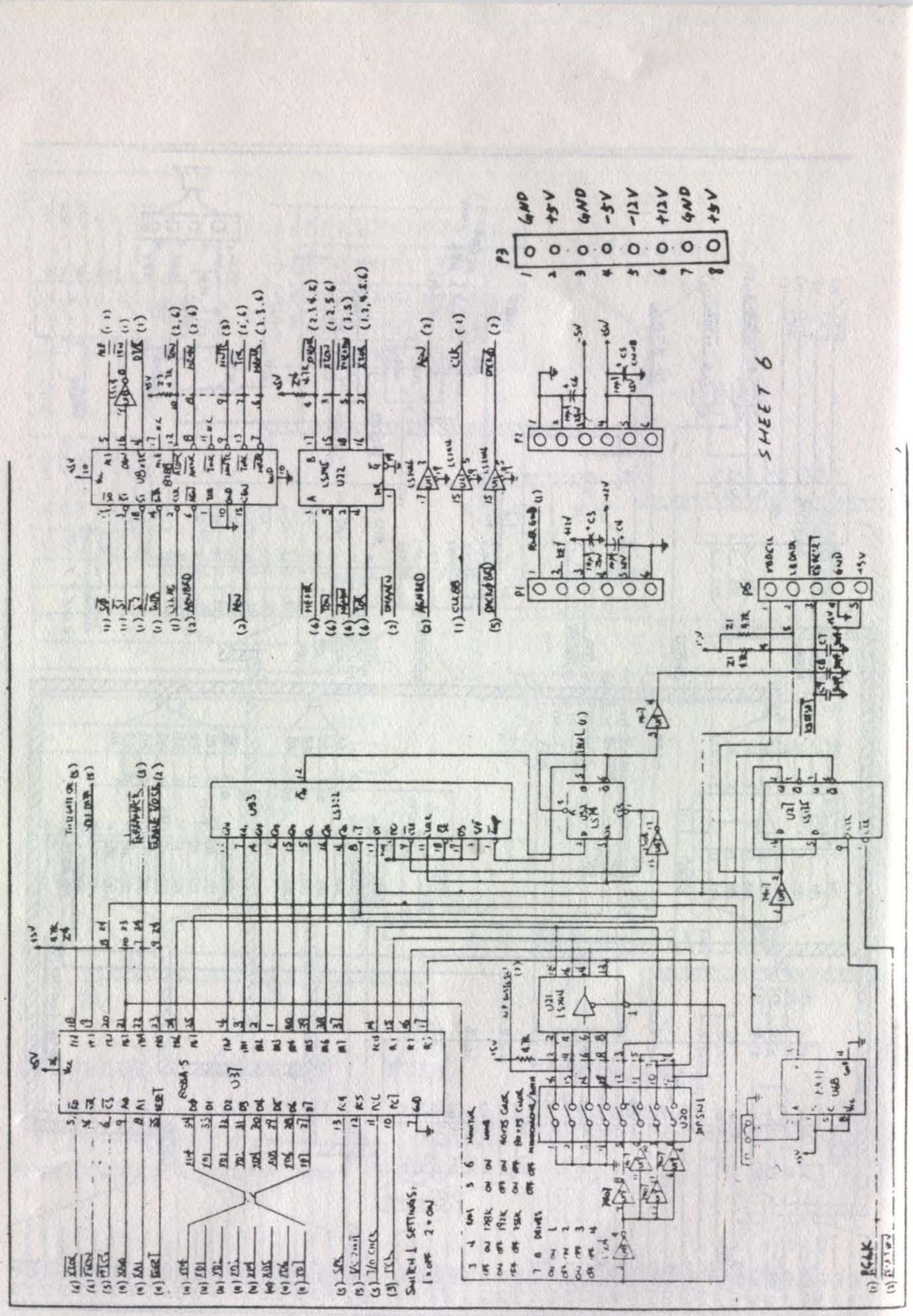


SHEET 3 256K DRAM



ROM/EPROM SELECTION	2764	27128	8K×8 RAM	32K×8 RAM
W1	ON	ON	ON	OFF
W2	OFF	OFF	OFF	ON
W3	ON	OFF	ON	OFF
W4	OFF	ON	OFF	ON
W5	ON	ON	OFF	ON
W6	OFF	OFF	ON	ON
W7	ON	ON	OFF	ON
W8	OFF	OFF	ON	OFF
W9	OFF	ON	OFF	ON
W10	ON	OFF	ON	OFF
W11	OFF	OFF	OFF	ON
W12	ON	ON	ON	OFF
U23	A	B	A	C





RAM SELECT

JP2		BANK		BANK	
A	B	0	1	2	3
ON	ON	4164	4164	4164	4164
OFF	ON	41256	41256	4164	4164
ON	OFF	4164	4164	41256	41256
OFF	OFF	41256	41256	41256	41256